High-Speed/Logic Gate Optocoupler (SFH67XX Series)

INTRODUCTION

The new SFH67XX series of high-speed optocouplers is capable of transmitting data rates up to 5 Mb/s typical and 2.5 Mb/s over the full specified operating temperature range. The combination of low input current (1.6 mA) and active logic-level output is a fit for nearly all logic applications where a galvanic insulation is necessary.

The SFH67XX series features positive logic with TTL output levels. For improved noise immunity the detector incorporates a schmitt-trigger stage.

The SFH6700/19 provides an enable input, which allows switching the output into the high ohmic state for bus applications.

For applications which need an open collector output, the SFH6705 is offered.The SFH6731 and SFH6732 are the dual versions. The two channels are free of crosstalk and interference.

To ensure a high common mode transient immunity of guaranteed 2.5 kV/µs at 400 V, the SFH671X/6732 series features an internal shield which consists of an additional ITO layer. The ITO (indium tin oxide) layer is an optically transparent but electrically conductive layer on top of the detector. The standard SFH670X series withstands 1.0 kV/µs at V_{CM} = 50 V.

The SFH67XX series is also available in an SMD version (option 7 and 9 with > 8 mm creepage and clearance distance).

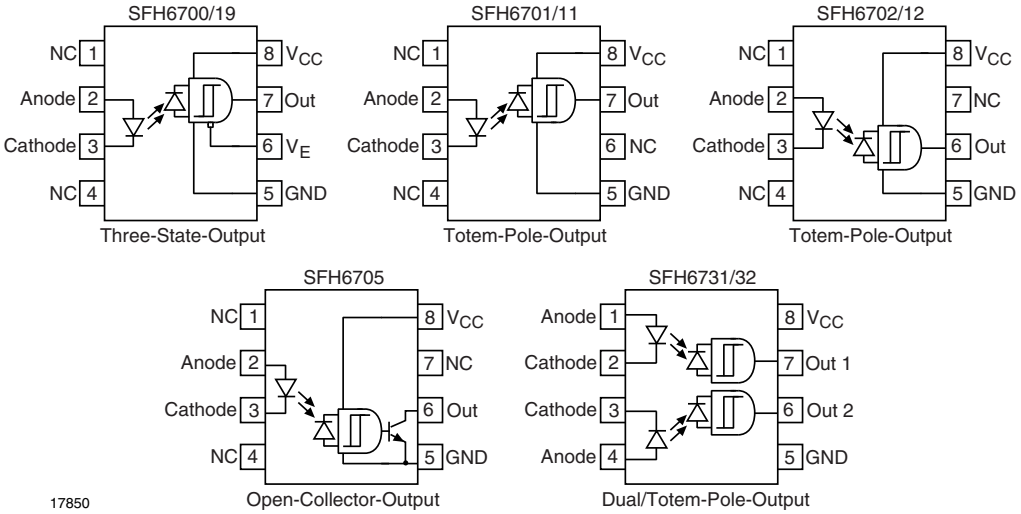

Fig. 1 - Variations in the SFH67XX Family

TABLE 1

LED	ENABLE	OUTPUT
SFH6700/19		
On	L	H
Off	L	L
On	H	Z
Off	H	Z
SFH6701/02/05/11/12/31/32		
On		H
Off		L

Truth table (positive logic)
H = logic high level, L = logic low level, Z = high ohmic state

DESIGN CONSIDERATIONS

The circuits shown below are intended to give the design engineer a guideline for logic family interconnection.

Input Circuitry

Below are stated the most common interface circuits which work for this coupler series.

Totem Pole Drive Circuits

Figures 2 and 3 are two of the most commonly used circuits. The designer chooses R_1 according to the equation:

$$R_1 = \frac{V_{OH} - V_F}{I_F} \quad \text{(valid for figure 2)} \quad (1)$$

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$$R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_F} \quad \text{(valid for figure 3)} \quad (2)$$

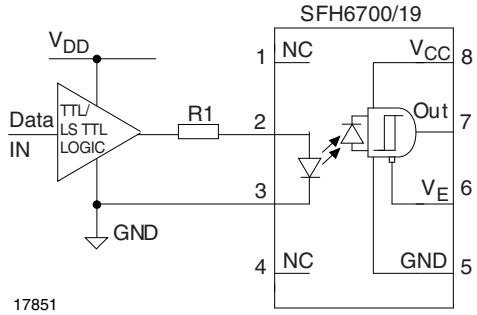

Fig. 2 - Series LED Drive

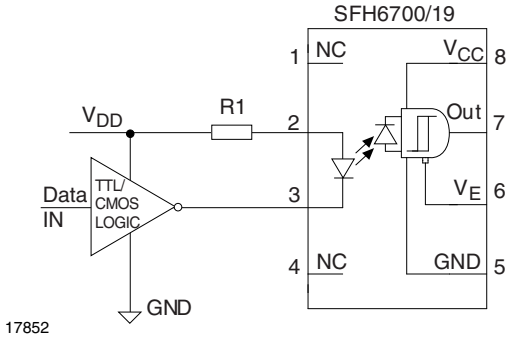

Fig. 3 - Series LED Drive

A good compromise between low power dissipation and symmetrical propagation delays with respect to some guard band is I_F = 3 mA. In some applications a speed-up capacitor (typically around 100 pF) across R_1 may be used to achieve faster switching times (please refer to the end of this section for details).

TABLE 2

FIGURE	LOGIC GATE (E.G.)	R_1 VALUE
2	74LS04	750 Ω
3	74LS04	1.10 kΩ
	74HCT04	1.10 kΩ

Typical values for R1 at V_{DD} = 5

Both circuits are simple and feature a minimal component count with low power dissipation. A logic source drive, as shown in figure 2, is not recommended due to speed and current limitations (especially in the CMOS logic family), and lower common mode transient immunity.

Due to the coupler's typically low input current threshold of 0.50 mA and the negative temperature gradient of the input current threshold (see figure 4), the output leakage current of the driver element at high temperatures may become an issue in certain applications where the circuit is operated at the upper temperature range.

For critical applications, where a high leakage current is expected, a shunt LED circuit, as shown in figure 5, is a good solution.

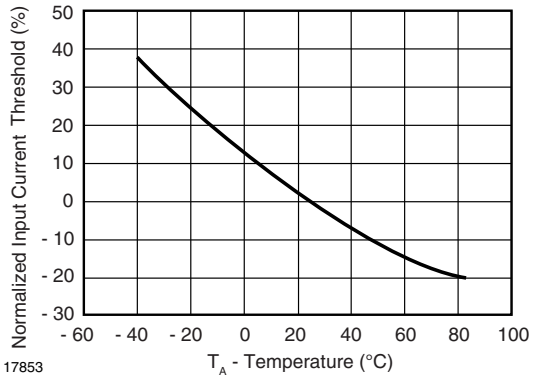

Fig. 4 - Typical Input Current Threshold (Normalized) vs. Temperature

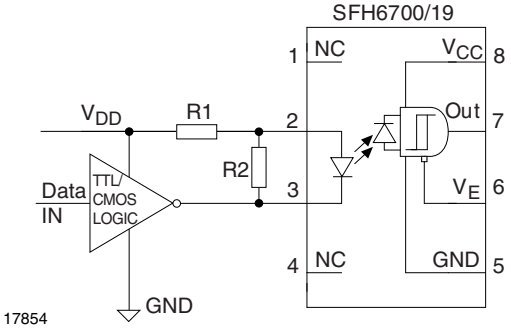

Fig. 5 - Shunt LED Drive Circuit with Leakage Current Protection

The resistor R_1 determines the forward LED current, and R_2 shunts the LED. The choice of R_2 depends on power dissipation considerations and the expected leakage current. The following equations can help designers determine the appropriate resistor values:

$$R_2 = \frac{V_{Fmax(LEDoff)}}{I_{Leak\ at\ Temp}} \cdot \frac{1V}{I_{Leakage}} \quad (3)$$

$$R_1 = \frac{V_{DD} - V_F - V_{OL}}{V_F + I_F R_2} \cdot R_2 \quad (4)$$

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TABLE 3			
V_{DD}	I_F	R_1 VALUE	R_2 VALUE
5 V	3 mA	1.0 kΩ	4.7 kΩ

Typical input circuit values to shunt around 250 µA away from the LED (according to figure 5)

A better way to handle leakage current is presented in figure 6.

This circuit provides excellent speed properties and leakage current protection. The silicon diode D_1 ensures that the current is only sourced by V_{DD} and is therefore not required for units driven by an open collector or open drain. The low forward voltage of D_1 ensures that the LED stays off at logic low. The equation to choose R_1 is:

$$R_1 = \frac{V_{DD} - V_F}{I_F} \quad (5)$$

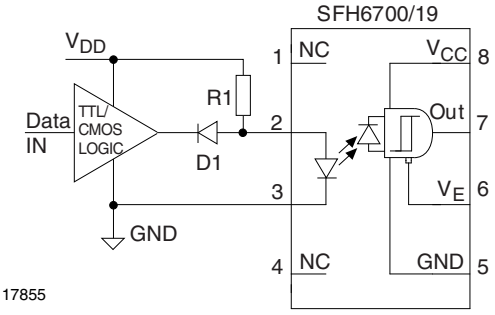

Fig. 6 - Logic Gate Shunt Drive Circuit

Open Collector Drive Circuits

A simple circuit, which also works for open collector drive circuits, has been presented in figures 3 and 5. In figure 5, the resistor R_2 represents a leakage current protection path.

A more efficient but more power-dissipating solution is presented in figure 7. This drive circuit provides good speed and protection against leakage currents. The resistor R_1 is chosen in accordance with

$$R_1 = \frac{V_{DD} - V_F}{I_F} \quad (6)$$

Refer to table 4 for some typical resistor values.

Note that leakage protection generally might only be an issue in some special applications.

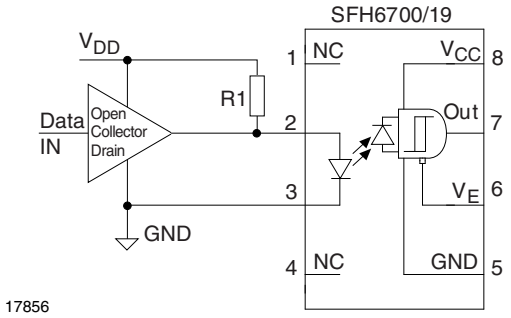

Fig. 7 - Open Collector/Drain Shunt Drive Circuit

TABLE 4		
V_{DD}	I_F	R_1 VALUE
5 V	3 mA	1.10 kΩ
10 V	3 mA	2.80 kΩ
15 V	3 mA	4.42 kΩ

Typical input circuit values for a circuit according to figure 7

Input Circuitry for Improved Switching Speeds

If switching speed is a concern, the use of a speed-up capacitor is a good solution. The resistor R_2 limits the peak transient current I_{Fpeak}, whereas R_1 and R_2 determine the current at steady-state operation. The equations and reasonable resistor values are printed below.

A reasonable value for the speed-up capacitor C_S is 100 pF.

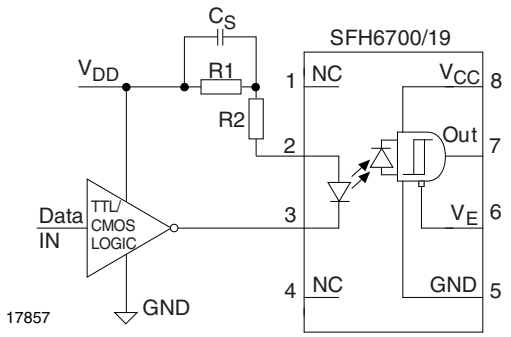

Fig. 8 - Series LED Drive with Speed-up Capacitor

The equations for the resistor values are:

$$R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_{Fpeak}} \quad (7)$$

$$R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_F} - R_2 \quad (8)$$

The maximum I_{Fpeak} for this transient is 50 mA for the SFH67XX series.

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TABLE 5			
V_{DD}	C_S VALUE	R_1 VALUE	R_2 VALUE
5 V	100 pF	1.0 kΩ	75 Ω

Typical input circuit values for a circuit according to figure 8

Output Circuitry

One advantage of the SFH67XX series is its easy connection to any logic system, because of the active output stage (totem pole/three state output). Either directly or via a pull-up resistor, all couplers can drive up to 16 LS TTL loads (4 TTL loads) easily. In general, a 0.1 µF bypass capacitor is strongly recommended for proper operation.

The SFH6700/19 with its three-state output fits best in bus applications because of the possibility to switch the couplers output into the high ohmic state (for a typical setup please refer to figure 28).

Drive Circuits for the Dual-Channel Devices

The SFH6731/32 can be driven as simply as the single channel devices.

All the above drive circuits and equations (1) to (8) can be adapted to drive the dual-channel devices. (The use of the dual-channel devices reduces the number of parts and the required board space.)

Interfacing to TTL/TTL-Compatible Logic

Interfacing the SFH67XX coupler to LS TTL or any other compatible logic is quite simple. The active output of this coupler eliminates the need for an external pull up resistor, and minimizes parts count and board space requirements. The typical connection is seen in figure 9. Even HCT logic can be interfaced this way.

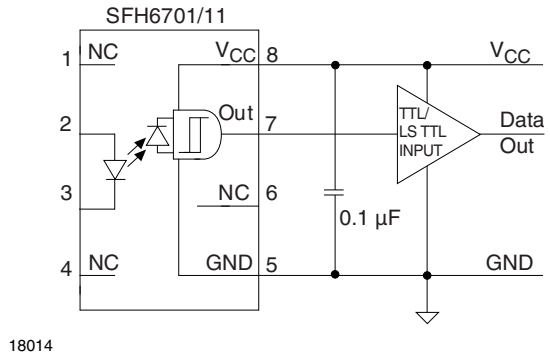

Fig. 9 - Interfacing the Coupler to TTL, LSTTL or Compatible Logic

Interfacing to CMOS Logic

To ensure reliable logic switching, a pull-up resistor between the output and V_{CC} is recommended (see Figures 11 and 12). For the HCT logic family, this pull-up resistor may be omitted, due to the matching switching level of the coupler's output and the HCT input.

There are three simple ways to connect CMOS logic to the SFH67XX coupler family:

- Using SFH67XX (totem pole) and a pull-up resistor (see figure 12)
- Using SFH6705 (open collector) and a pull-up resistor (see figure 11)
- Using an HCT logic device (see figure 10)

Using an HCT device is the simplest and most convenient solution to eliminate the external pull-up resistor (see figure 10). The designer doesn't have to worry about power consumption, rise times, or system speed.

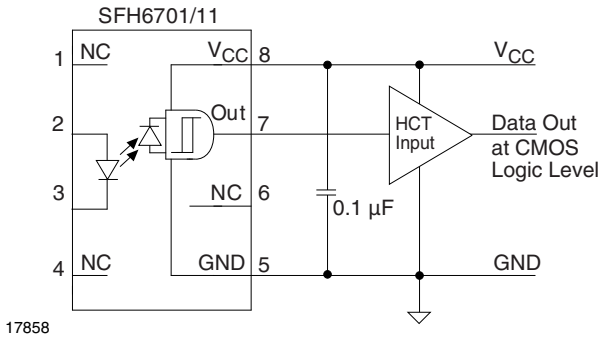

Fig. 10 - Interfacing to CMOS Logic Level via a HCT Device

Using the open collector device, as in figure 11, requires an external pull-up resistor R_P. To determine the correct value of this pull-up resistor, use following equations:

$$R_{Pmin} = \frac{V_{CCmax} - V_{OLmin}}{I_{OLmax} + n \cdot I_{IL}} \quad (9)$$

where $n \cdot I_{IL}$ represents the total load current at low level V_{OL}. (To ensure $V_{OLmax} < 0.5$ V over temperature I_{OLmax} should be set not higher than 6.4 mA).

The maximum R_P value can be determined by:

$$R_{Pmin} = \frac{V_{CCmin} - V_{IHmin}}{I_{OHmax} + n \cdot I_{IH}} \quad (10)$$

In CMOS applications however, where I_{IH} is in the µA region, the limiting factor can also be determined by the maximum allowable rise time t_r (500 ns for HC logic). The equation

$$V_H = V_{CC}\left(1 - e^{\frac{-t}{R_P C_L}}\right) \quad (11)$$

leads to

$$R_{Pmax} = \frac{-t_r}{C_L \cdot 1n\left(1 - \frac{V_{IHmin}}{V_{CCmin}}\right)} \quad (12)$$

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in which C_L represents the total capacitance of the load, including the coupler (which is around 6 pF).

The resistor value is a compromise between the requirement of power dissipation and switching speed. A low R_P produces symmetrical and fast switching times but results in a higher power dissipation. Reasonable values are shown in table 6.

Details of the relationship between the rise time t_r and the pull-up resistor R_P/load capacitance C_L are shown in figure 14.

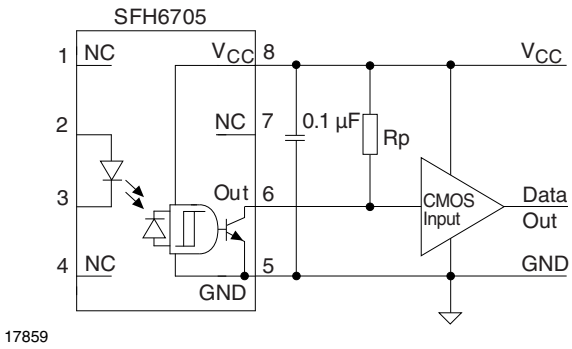

Fig. 11 - Interfacing SFH6705
(Open Collector Output) to CMOS Logic

By using a totem pole device, the equations (9) and (10) are also valid, but the pull-up resistor has only to bring up the voltage difference between V_{OH} ($\approx V_{CC}$ - 1.8 V) and the input switching limit, e.g. 3.5 V for HC logic, which makes a ΔV of 0.3 V. This allows the use of a higher R_P which results in lower power consumption.

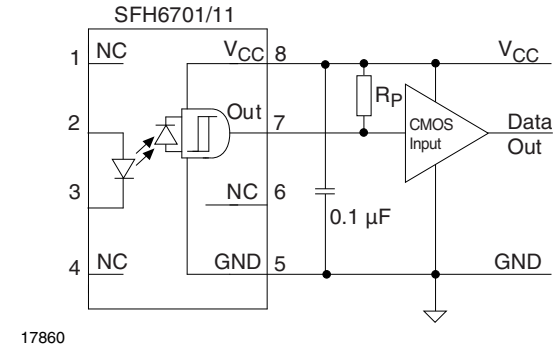

Fig. 12 - Interfacing SFH67XX (Totem Pole Output) to CMOS Logic

TABLE 6		
V_{CC}	R_P (OPEN COLLECTOR)	R_P (TOTEM POLE)
5 V	820 Ω	1.10 kΩ

Typical values for R_p by connecting to CMOS logic (according to figures 11 and 12).

Note that generally the R_P value has a negligible influence on the delay time t_d, but it strongly determines the rise time, especially for the open collector type.

Interfacing to 3.3 V Level

Interfacing to the 3.3 V logic families (e.g. AC, AHC, or HC) is quite easy, and presented in figure 13.

If the totem pole/three-state coupler is operated with V_{CC} = 5 V, then the output “high” level of the coupler, which is then typically 3.2 V, matches perfectly with the 3.3 V logic input levels. In general, the output “high” voltage can be determined by $V_{OH} \approx V_{CC}$ - 1.8 V. (Even with V_{CC} = 5.0 V ± 10 %, the output voltage is within the limits, and is guaranteed to be higher than 2.4 V over temperature to fulfill the 3 V logic requirement).

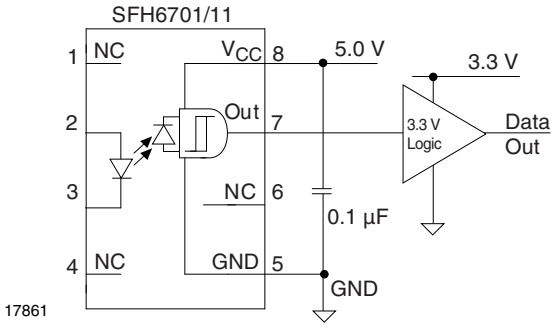

Fig. 13 - Interfacing to 3.3 V Logic with V_{CC} = 5 V

Interfacing to other Levels

If shifting to any other level is intended (e.g. 2.5 V logic, like the ALVC or ALVT series), the SFH6705 with its open collector output is qualified. R_P works as a pull-up resistor to ensure the proper logic high level. The basic principles are the same as described in the section “interfacing to CMOS logic” in equations (9) to (12).

Pull-Up Resistor Considerations for the Open Collector Type SFH6705

As previously mentioned above, the pull-up resistor has to be chosen in accordance with the equations (9), (10), and (12). Figure 14 plots the expected rise time t_r versus the time constant $\tau = R_P \times C_L$. Unlike the rise time t_r, the fall time t_f is mostly independent of R_P and around 5 ns.

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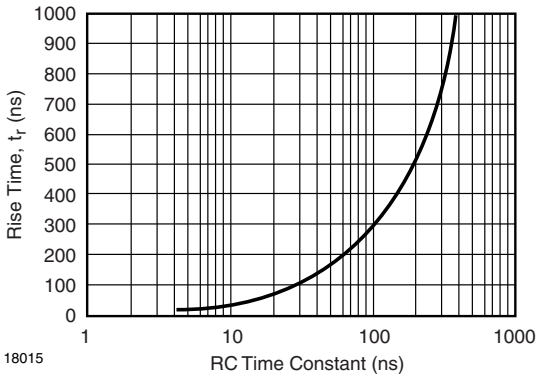

Fig. 14 - Typical Rise Time vs.
Load for V_{CC} = 5 V (Test Circuit See Figure 15)

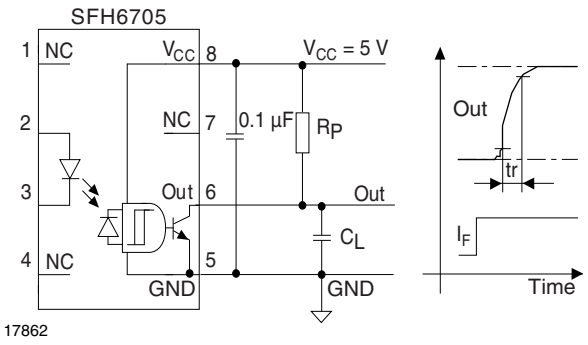

Fig. 15 - Test Circuit for Rise Time t_r vs. Time Constant

COMMON-MODE TRANSIENT IMMUNITY (CMTI)

The SFH6711/12/19 feature a guaranteed common mode transient immunity (CMTI) of 2.5 kV/µs at 400 V. This is achieved by using a faraday shield which is transparent to infrared light, but electrically conducting. This shield prevents the photodiode from being turned on by common-mode transients.

In general there are some design rules to achieve a high CMTI. These recommendations are especially important for low LED drive current devices, like the SFH67XX series:

- Connect the unused pins 1 and 4 to the virtually grounded input potential (either GND or V_{DD}).
- Minimize stray capacitance.
- Avoid long distances between LED input circuit and coupler.
- Choose an appropriate high LED forward current to improve CM_H (common mode transient immunity at logic "high" level).

A layout which implements these hints is seen in figure 16. Note that this layout reduces creepage and clearance distance as well.

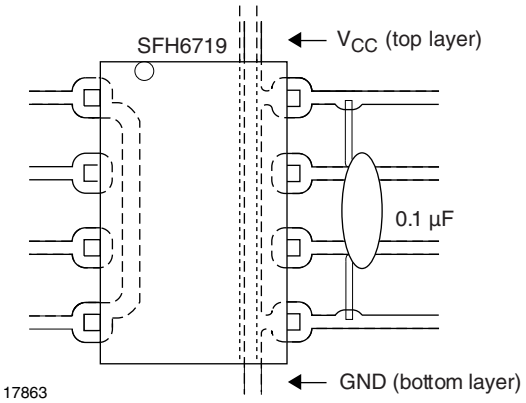

Fig. 16 - Principle Board Layout for
Enhanced CMTI (Fits to Schematic in Figure 18)

A circuit which enhances CMTI safety is shown in figure 17.

The diode D_1 is intended to sink parasitic current, which is caused by stray capacitance, away from the LED to prevent a false turn-on.

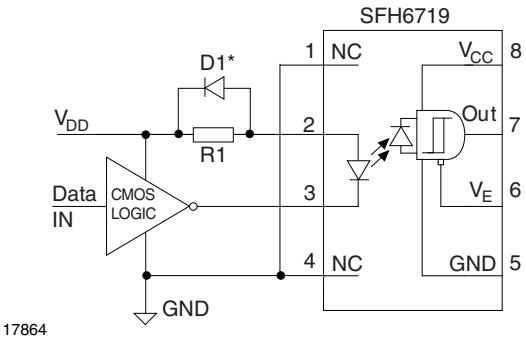

Fig. 17 - Input Circuitry for Improved CMTI

* Diode D_1: Any signaling diode

Another input circuit for high CMTI is shown in figure 18.

The transistor shunts the LED in the off-state and prevents a false turn on. This circuit tolerates very high common mode transients in the LED off-state. An improvement in the LED on-state can be reached by choosing a high I_F current. For V_{DD} = 5 V, R_1 is typically around 1.1 kΩ.

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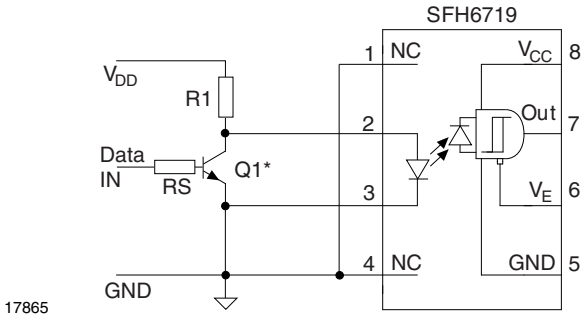

* Transistor Q1: Any switching transistor (e.g. 2N2222)

Fig. 18 - Input Circuitry for High CMTI

A common way to achieve ultra-high CMTI is presented in figure 19.

The balanced input impedance principle works with four resistors, $R_1 = R_2$ and $R_3 = R_4$. R_1 and R_2 are used to minimize any noticeable LED current when the transistor is on. To achieve maximum performance, the stray capacitance from anode or cathode to the output side of the coupler has to be kept as low as possible.

Reasonable values with Q_1 = 2N2222 are $R_3 = R_4$= 510 Ω and $R_1 = R_2$ omitted. Note that R_1 and R_2 can be omitted, depending on the V_{CE} of the transistor Q_1.

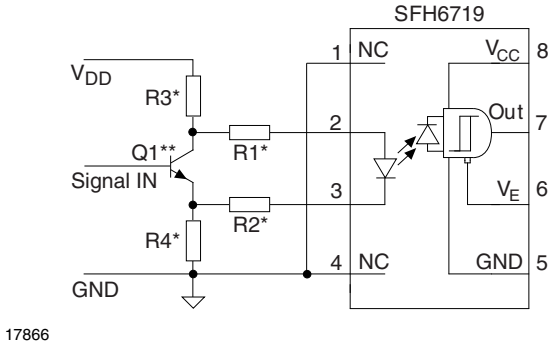

Fig. 19 - Balanced Input Impedance Circuitry

* Resistor $R_1 = R_2$ and $R_3 = R_4$: To achieve a balanced input impedance

** Transistor Q_1: Any switching transistor

DYNAMIC OPERATION

The SFH67XX series of active pull-up outputs offer a guaranteed maximum propagation delay time of 300 ns over temperature and as well as a guaranteed 2.5 Mb/s data rate over temperature.

Pulse Width Distortion

Pulse width distortion (PWD) is defined as the difference between t_{PHL} and t_{PLH} (PWD = $|t_{PHL} - t_{PLH}|$). This value is important in applications where symmetrical switching times are required, e.g. in systems which are based on pulse width modulation. In transmission systems, the PWD should not exceed 30 % of the minimum propagation delay time. At I_F = 3.0 mA LED forward current, the SFH67xx has a typical PWD of around 20 ns over temperature, which corresponds to a maximum PWD of 20 %. Note that the use of a speed up capacitor decreases t_{PLH} but might increase the PWD.

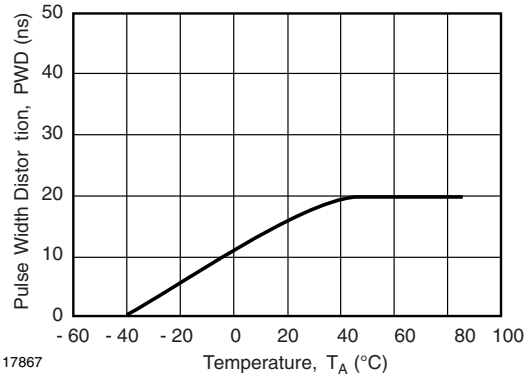

Fig. 20 - Typical Pulse Width Distortion over Temperature at I_F = 3 mA (Test Circuit See Figure 24)

Propagation Delay Skew

Propagation delay skew (t_{PSK}) is the difference between the minimum propagation delay, either t_{PHL} or t_{PLH}, and the maximum propagation delay, either t_{PLH} or t_{PHL}, between any SFH67XX coupler under the same operation conditions. Propagation delay skew is therefore an important value for parallel data transmission, where synchronized data is needed.

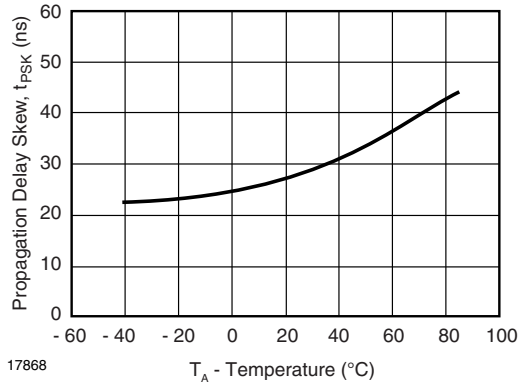

Fig. 21 - Typical Propagation delay Skew over Temperature at I_F = 3 mA (Test Circuit See Figure 24)

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In logic circuits, the overall PWD and t_{PSK} are determined by all input and output logic gates in the signal path. To minimize the overall PWD, two identical couplers may be used as shown in figure 22. But the minimum PWD is achieved at the cost of a higher overall propagation delay.

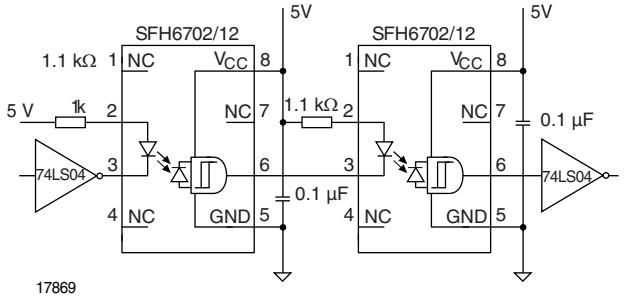


Fig. 22

Eye Pattern Diagram

A typical eye pattern diagram for 5 Mb/s data transmission is presented in figure 23. The eye pattern testing was done with a pseudo random data sequence (NRZ coding).

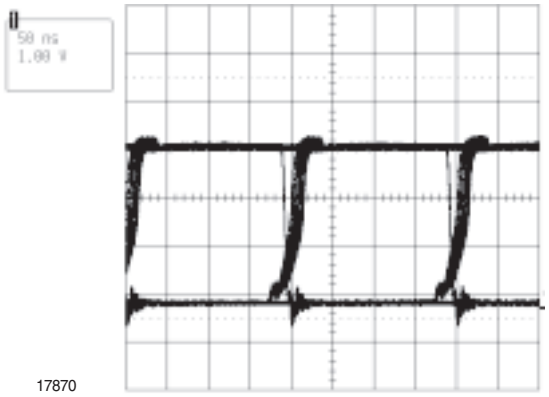


Fig. 23

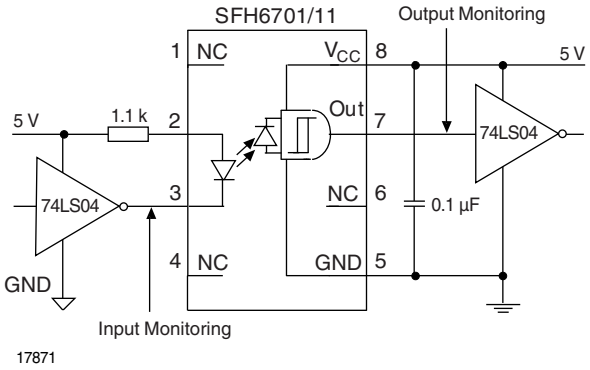


Fig. 24

DESIGN IDEAS

Optocouplers are commonly used as an interface between two circuits, where galvanic insulation is required, either to protect humans or sensitive electronic equipment.

Based on this requirement, some designs are presented below, which use the SFH67XX series.

IGBT/IPM Driver

The SFH67XX series can be used as a fast driver for intelligent power modules (IPMs) using IGBT or MOSFET technology.

The SFH67XX optocoupler series provide level shifting and galvanic insulation and is therefore the ideal interface to the control logic.
With its guaranteed minimum 2.5 kV/µs at 400 V common mode transient immunity, the SFH671X also fulfills enhanced switching requirements.

Switching Loads

The SFH67XX series can easily handle currents up to 25 mA_{DC} and voltages up to 15 V. Figures 26 and 27 show how it can handle loads which are beyond these limits.

In figure 26, R_1 is used as a pull-up resistor and the load current is handled and limited by the external transistor Q_1. Unlike figure 27, the schematic in figure 26 is qualified to support both high voltages and currents. The 5 V power supply might be raised up to 15 V to achieve a proper V_{GS} voltage to turn the transistor fully on.

The combination of the SFH67XX series with logic level power transistors provides a fast-switching solution that helps to reduce parts count.

High-Speed/Logic Gate Optocoupler (SFH67XX Series)

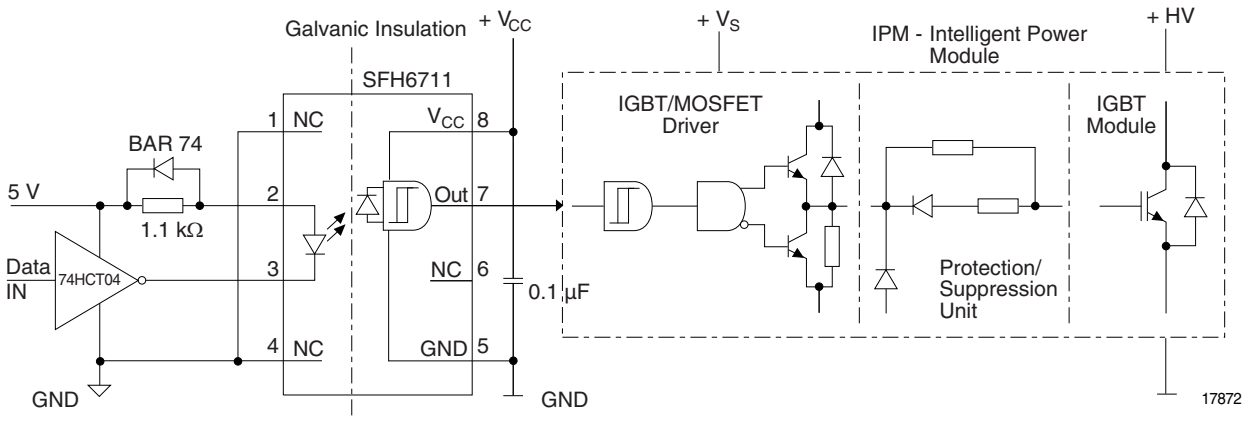


Fig. 25

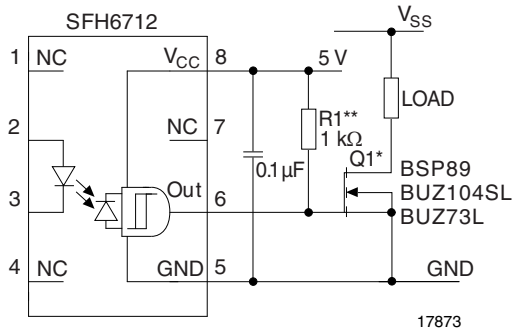


Fig. 26

* Transistor Q_1: Any n-channel enhancement-mode transistor

** Resistor R_1: R_1 might be omitted, depending on the necessary V_{GS} of Q_1 to turn Q_1 fully on

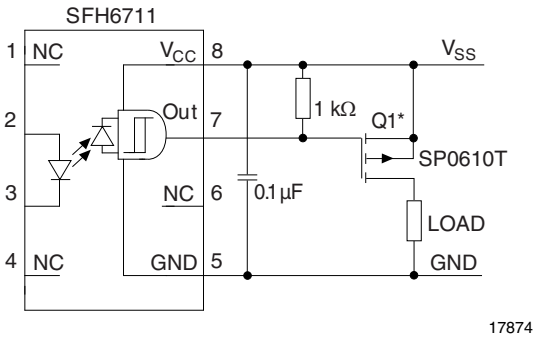


Fig. 27

* Transistor Q_1: Any p-channel enhancement-mode transistor

Time Multiplexed Bus Line Access with Optical Insulation Barrier

The schematic in figure 28 shows the use of a common data bus line with 4 independent data lines in time multiplexing mode. The 2-line to 4-line address decoder selects one of the 4 data lines by enabling the output, whereas all the other outputs remain in the high ohmic state.

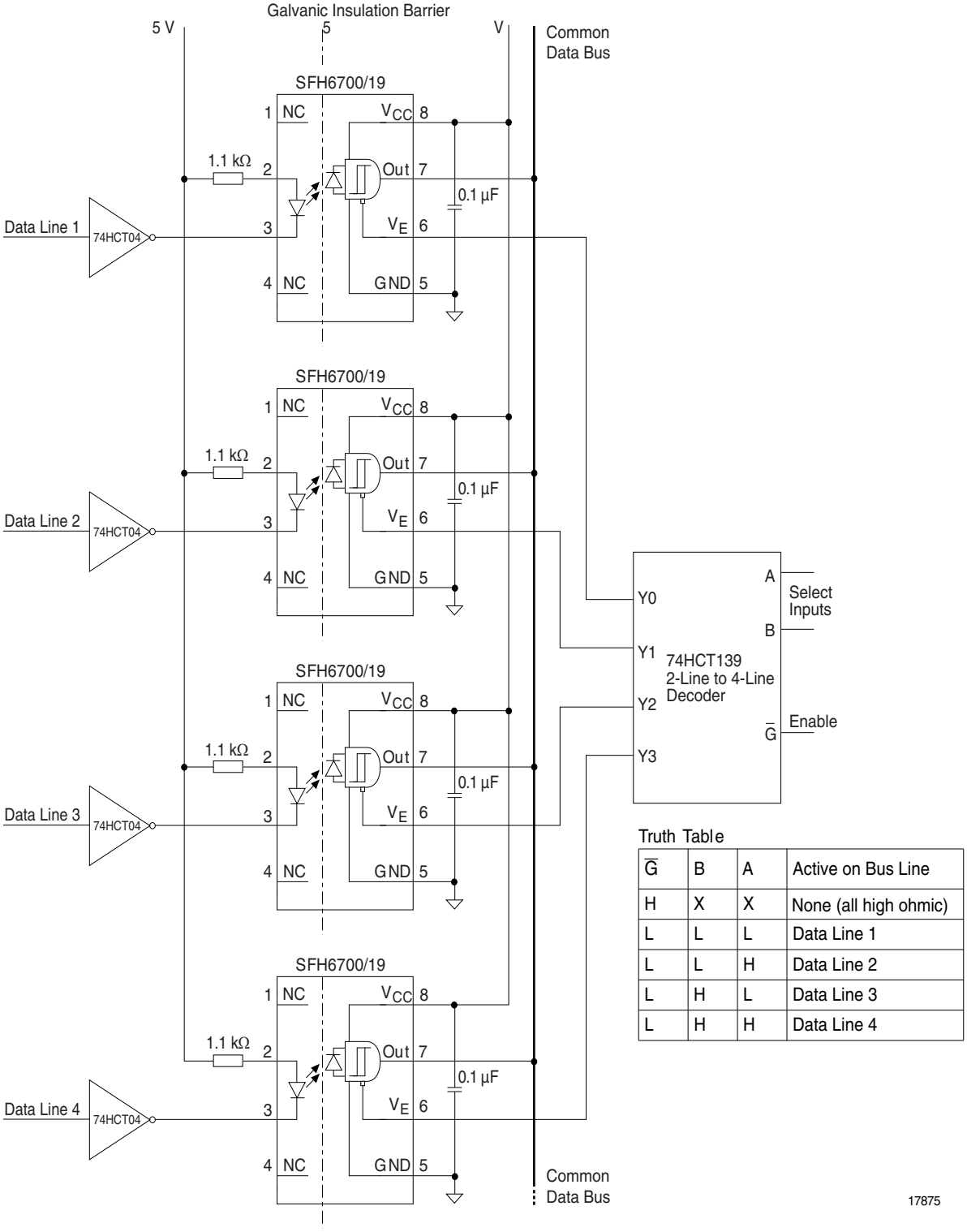
Opto-Insulated DAC Interface

When galvanic insulation in digital-to-analog-conversion or analog-to-digital-conversion systems is required, the SFH67XX series is a good choice for an interface.

Setups like the one in figure 29 provide a fast and part saving insulation barrier. The low propagation delay skew of the SFH67XX devices makes them ideal for use in parallel data transfer. The SFH67XX series provide an optimal interface solution for the SAB 80 C167/C165 micro-controllers by supporting the 5 Mb/s data rate at a 20 MHz CPU clock.

APPLICATION NOTE

High-Speed/Logic Gate Optocoupler (SFH67XX Series)



Truth Table

$\overline{G}$	B	A	Active on Bus Line
H	X	X	None (all high ohmic)
L	L	L	Data Line 1
L	L	H	Data Line 2
L	H	L	Data Line 3
L	H	H	Data Line 4

Fig. 28 - Typical Setup for a Common Bus Line with 4 Different Lines in Time Multiplex Mode

APPLICATION NOTE

High-Speed/Logic Gate Optocoupler (SFH67XX Series)

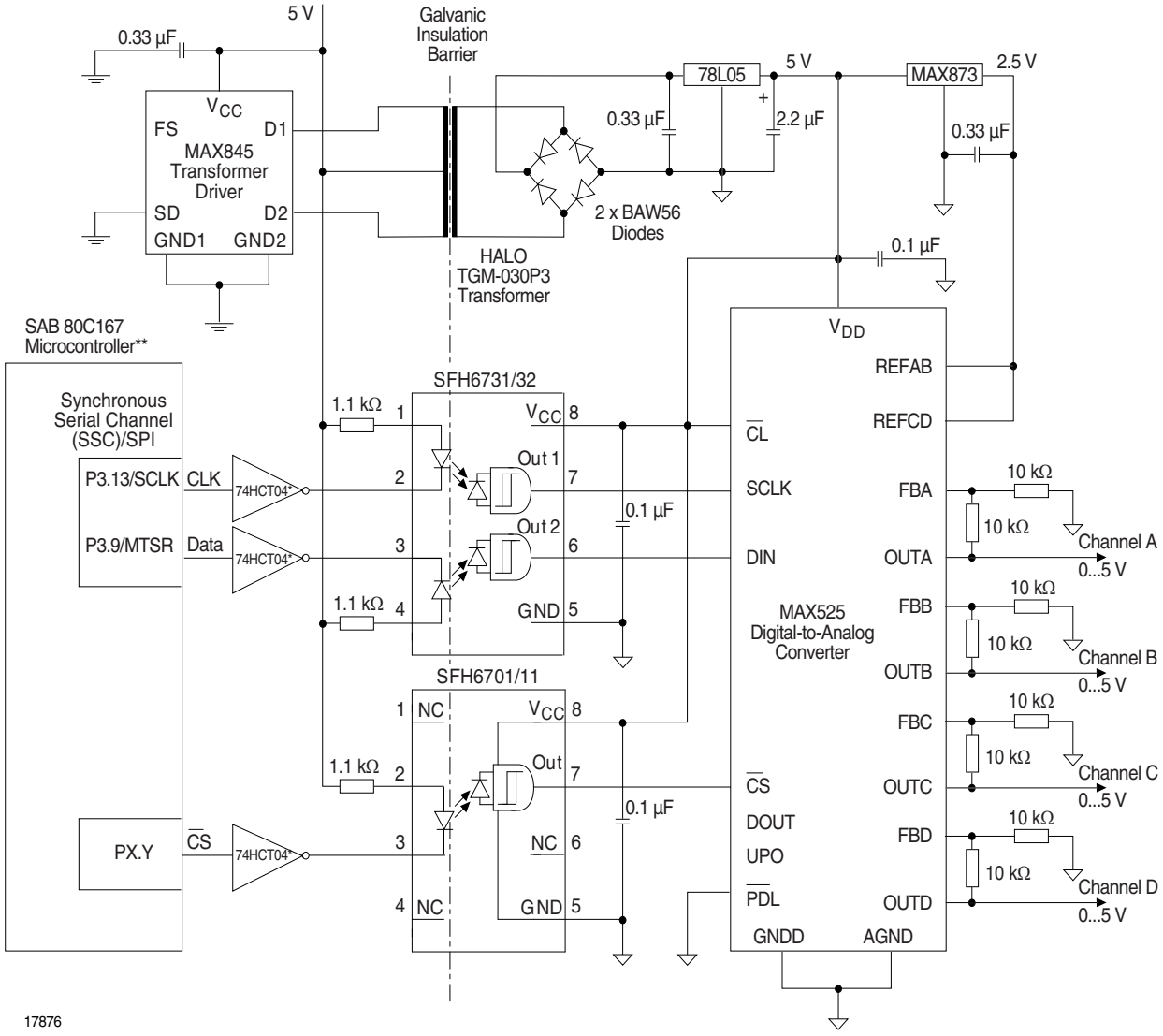


Fig. 29 - Fully Galvanic Insulated Digital-to-Analog-Conversion System (4 Channel DAC)

* Inverter 74HCT04 is used to allow 3 mA LED current

** Any C16X micro-controller can be used

APPLICATION NOTE