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How to Deal with TRENCHSTOP™ 5 IGBT in Power Applications

by Infineon

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While the main market for power applications is still seen in the drives segment, other segments focusing on higher switching frequency ranges gained importance. UPS, Photovoltaic, and Welding Applications, to name a few, have grown significantly in size in recent years.

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In order to respond to the respective needs, Infineon recently developed and released the TRENCHSTOP™ 5 IGBT technology especially focusing on the above mentioned field of applications.

This technology enables power system manufacturers to achieve much higher switching frequencies compared to previous Trench Field-Stop IGBT technologies.

This article provides some basic information and general hints on how to deal with Infineon's TRENCHSTOP™ 5 IGBT technology in typical power applications improving performances without impacting the product reliability.

TRENCHSTOP™ 5 main characteristics and performances Starting from the former HighSpeed3 technology, Infineon's TRENCHSTOP™ 5 technology (TS5) allows for achieving unparalleled switching frequencies. This improvement has been possible thanks to the features, implemented within this new technology. They are:

- faster switch-off capability
- lower forward voltage $V_{CE(sat)}$ and lower turn-on losses E_{on}
- reduced device input capacitance and gate charge.

Furthermore, to respond more specifically to customer needs, the TS5 technology has been divided into the two different variants F5 and H5, respectively:

- F5 (IK_40N65F5) is the extremely fast version, best fit in combination with SiC diodes; needs split R G(on) and R G(off) and predestined to be used in applications having excellent layout routing with a total stray inductance less than 20...30nH.

- H5 (IK_40N65H5) is the fast version, intended for industrial applications like Welding, UPS and Solar and best to be used in systems having a good layout routing with a total stray inductance in the commutation loop less than 30...60nH. It can be used in combination with ultrafast silicon diodes.

Table 1 shows a summary of the main parameters of the F5 and H5 IGBT variants compared to former HighSpeed3 IGBT.

Parameter		Conditions	Values			Unit
			IK_40N60H3 High Speed 3	IK_40N65F5 TS5 - F5	IK_40N65H5 TS5 - H5	
Static Characterist.	BV_{CES}	V_{GE}=0V, I_C=2mA, Min.	600	650	650	V
	I_C	V_{GE}=15V, T_{vj}=25°C, I_C=40A	80	74	74	A
	I_C	V_{GE}=15V, T_{vj}=100°C, I_C=40A	40	46	46	A
	$V_{CE(sat)}$	I_C=40A, V_{GE}=15V, RT, Typ	1,95	1,65	1,6	V
	$V_{GE(th)}$	V_{CE}=V_{GE}, I_C=500µA	5,1	4	4	V
	g_{fs}	V_{CE}=20, I_C=40A	24	50	50	S
Input Char.	C_{ies}	V_{CE}=20V, V_{GE}=0V, f=1MHz	2,19	2,5	2,5	nF
	C_{oes}		112	50	50	pF
	C_{res}		64	9	9	pF
	Q_G	V_{CC}=480V, I_C=40A, V_{GE}=15V	223	95	95	nC
Dynamic Charact.	$t_{d(on)}$	V_{CC}=400V, I_C=20A, T_C=25°C, V_{GE}=0V/15V, $R_{G(on)}$=$R_{G(off)}$=15Ω, L_σ=45nH, C_σ=40pF, Typ.	19	21	21	ns
	t_r		33	10	11	ns
	$t_{d(off)}$		197	140	140	ns
	t_f		21	8	8	ns
	E_{on}		610	300	270	µJ
	E_{off}		290	130	160	µJ

Table 1: Comparison between 600V 40A HighSpeed3 IGBT and 650V 40A H5/F5 IGBT variants in TRENCHSTOP™ 5 technology

A change in key parameters shows up in a reduction of rise and fall times down to 30%, accompanied by a gate charge decrease of 60%. The device's capacitance C oess is now reduced up to one third and C ress is diminished by about 85%.

Switching characteristics

High switching speed technology does not automatically mean best performances in every application. It should be considered that in several cases, especially when using TS5 IGBT solutions, it is not possible to replace former high-speed IGBT technologies 1:1 with TS5, without providing any layout improvements.

To get the highest benefits from these fast switching technologies, PCB, DCB or IMS layout designs must have extremely narrow current compensation paths to get the lowest parasitic. The free-wheeling diode (FWD) and the gate loop have to be optimized as well. Moreover, the isolation materials and related thicknesses must be carefully selected to avoid EMI related issues and limitations on the maximal achievable dv/dt, which would limit the maximum switching frequency accordingly.

In situations where these two factors are not considered or underestimated, fast switching technologies may even lead to higher losses and limitations, both in turn-on and in turn-off.

Turn-off improvements

One third of the fall time than previous HighSpeed3 IGBTs, per same output current in the same application leads to three times higher di/dt. This effect may induce over-voltages which lead to additional power losses and modification of the trajectory in the switching locus.

An application with 50nH parasitic inductance, previously driven at 1kA/µs, with TS5 may experience a di/dt as fast as 3kA/µs, leading to a voltage overshoot of 150V. In this case, the 50V added to the minimum $V_{(BR)CES}$, now rated 650V, helps to reduce the electrical stress due to voltage overshooting. Practical countermeasures to be used in the design in order to avoid undesired effects during turn-off include:

- **PCB, DCB or IMS have to be designed with very good current compensation loops.**
  A system design having stray inductance L_σ < 30...50nH, including leads in case of discrete device, is strongly recommended.

V_{GE} [V]	R_G [Ω]	Reference: V_{GE}=+15V/0V, R_G=10Ω	
		E_{off} difference [%]	ΔV overshooting difference [%]
+15V / 0V	18	+10.9	-22.6
+15V / -5V	18	-40.8	-48.4
+10V / -12V	56	-32.8	-53.6
+10V / -12V	89	+11.5	-63.9

Table 2: E_{off} losses comparison in a layout having a L_σ=56nH at different driving conditions

- **Introduction of Clamping Circuits**
  Capacitor clamping or also other alternative clamping structures, placed as close as possible to the device, are strongly recommended. Energy recovery clamping or C-D clamping structures with SiC diode are possible options. An example of DCB substrate with integrated clamping structure and related waveform improvements are shown in Fig. 1.a and b.

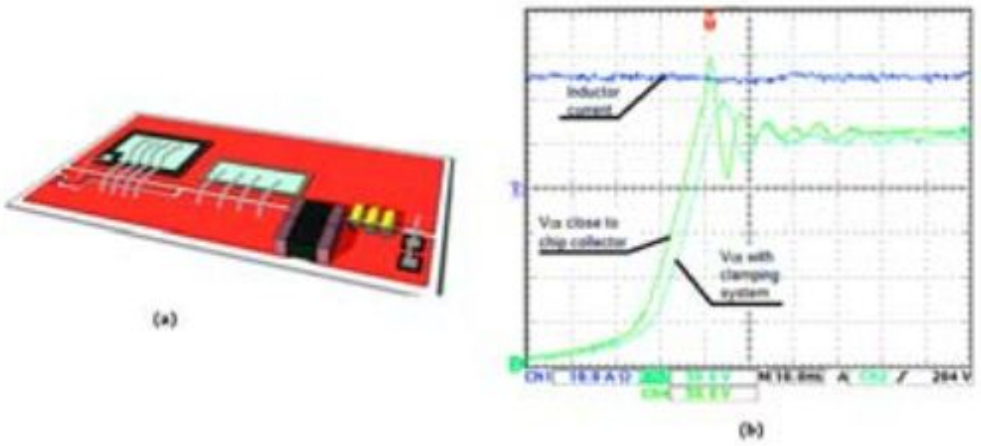

Figure 1: Recommended solution with a possible clamping network to be placed as close as possible to the IGBT/FWD. 40A/650V TS5 F5 IGBT turn-off at T_c=25°C. V_{CE} measured with clamping system (cyan, 50V/div). V_{CE} in standard conditions, R_G=10Ω, V_{GE}=15V/0V

- **Introduction of Passive Gate Network**
  Splitting the gate resistance into $R_{G(on)}$ and $R_{G(off)}$ usually helps to relief stress and avoid further power losses.
  Eventually introduction of a small gate-emitter capacitance improves control ability, but oscillations must be kept at tolerable levels and in this case a damping series resistor R_{GE} might be helpful.
  In some situations, a small ferrite beat directly at the gate pin might help to filter undesired oscillations at very high frequencies.
- **Negative gate voltage with a slightly increased $R_{G(off)}$.**
  In case of relatively large parasitic inductance, a good compromise might be to increase $R_{G(off)}$ and to drive at the gate using negative voltage.
  E_{off} and ΔV overshooting for an IKW40N65H5 was measured in a welding machine application at I_c = 20A, Tamb = 25°C, V_{CE} = 360V, L_σ = 56nH. In Table 2, are listed the results at different V_{GE} and R_G values, using per reference E_{off} = 131µJ and a voltage overshooting ΔV = 97V resulting from a condition of V_{GE} = +15V/0V and R_G = 10Ω . Within this approach and using proper $R_{G(off)}$ vs. V_{GE} compromise, it is possible to reduce E_{off} and to reduce voltage overshooting, also avoiding parasitic turn-on.

Turn-on improvements

IGBTs historically suffered from high E_{off}. But now, TS5 offers a dramatic reduction of E_{off} losses. Therefore, the attention of the designers is recently focusing on E_{on}. One third of the rise time than previous HighSpeed3 IGBT technology may reflect in oscillations and large I_{RRM} on the paired FWD. In some conditions, this may lead to higher E_{on}, EMI and RF emissions. Practical countermeasures to be used in the design in order to avoid undesired effects during turn-on include:

- **Selection of a FWD with optimized reverse recovery performance.**
  Test results using the same TS5 F5 IGBT at different diode combinations can be verified in Figure 2.c.

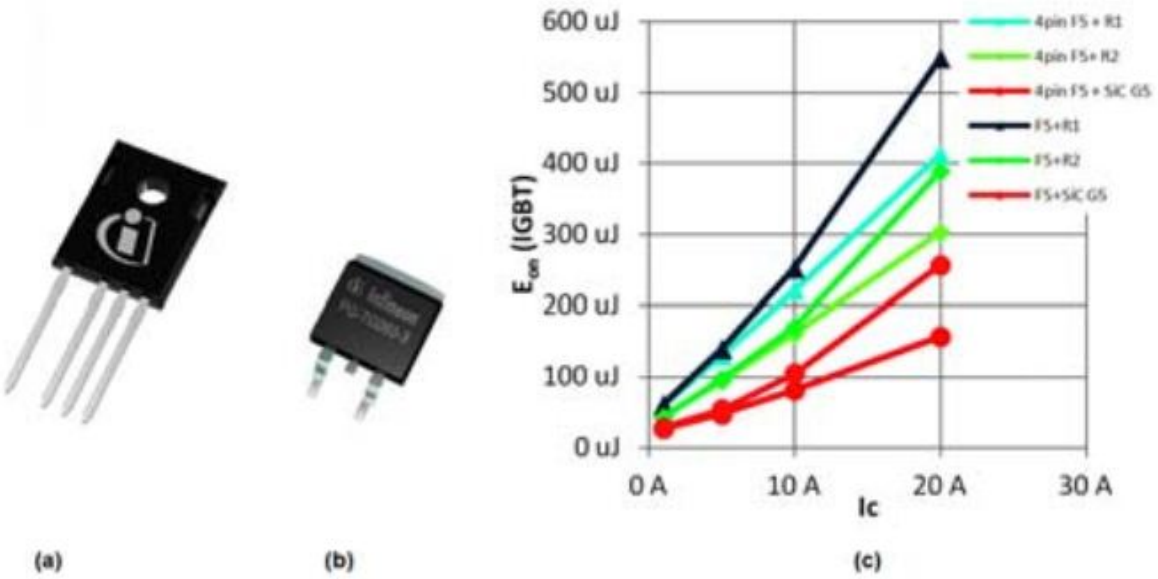

Figure 2: (a) TO-247-4 Leads package, (b) TO-263 (D^2Pak) package, (c) Turn-on switching losses of a 650V 40A IGBT F5 device at T_C=100°C, R_G=10Ω and V_{GE}=15V at different combinations of package and FWD (R1=Rapid 1, R2=Rapid 2, SiCG5=Silicon Carbide diode 5th Generation).

- **Splitting the gate resistance in $R_{G(on)}$ and $R_{G(off)}$.**
- **Selection of the proper package when using TS5 in discrete components.**
  4-Leads-PTH and SMD packages at high current ratings as shown in Figure 2.a and Figure 2.b should be preferred since offer great benefits in $t_{(on)}$.
- **Shorten the IGBT/FWD power loop. Especially in DCB and IMS module design.**
- **Use auxiliary emitters, especially in DCB or IMS design, mainly for the top side IGBT.**
  Figure 3 shows an example of DCB design which uses an auxiliary emitter on the top side IGBT.

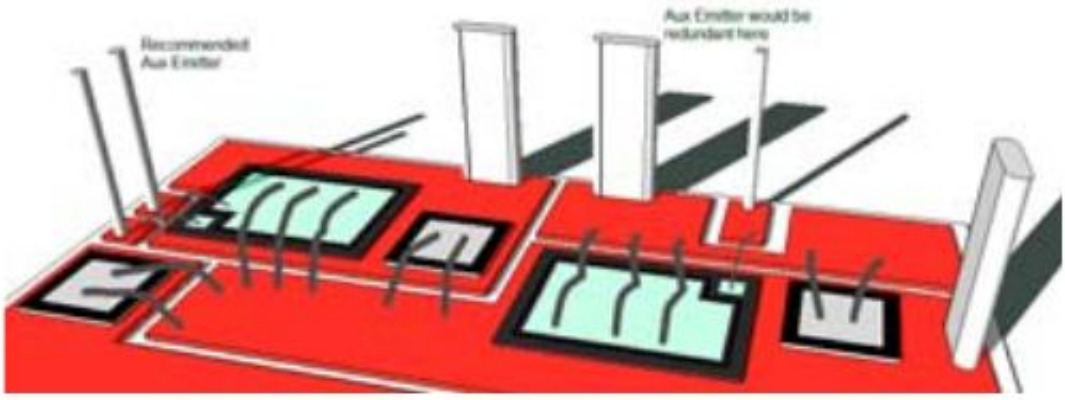

Figure 3: Example of a DCB layout with, and without, auxiliary emitter terminal

- **Use an integrated clamping circuit very close to the device, especially on DCB and IMS solutions.**
- **Avoid the use of double stitch or butterfly bonding between IGBT and FWD, rather prefer solutions as depicted in Figure 1.a wherever possible.**

- **Multiple paralleling is not recommended, but in case of necessity, use separate gate network and buffers close to the gate of the device.**

Introduction of the above mentioned countermeasures allow to fully exploiting the potential and the high performances of Infineon’s new TRENCHSTOP™ 5 IGBT technology.

Rating: 6.0/**6** (1 vote cast)